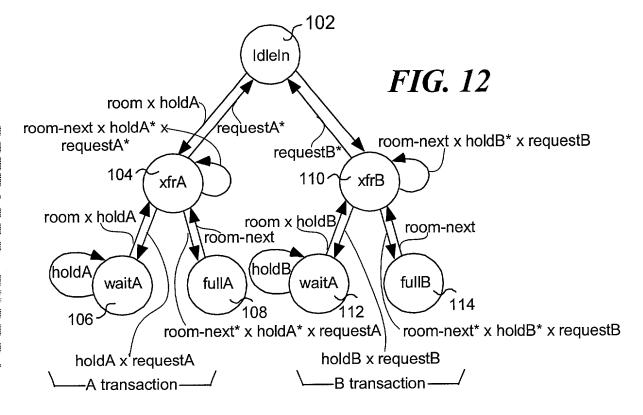
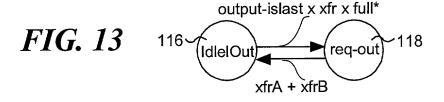
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24175	time.	Menne.

register management flip-flops			data buffer registers	
inputis 1	reg1last	reg1full	reg 1	
outputis 1	reg2last	reg2full	reg 2	

FIG. 11



transaction = IdleIn*
room-next = empty + xfr
room = reg1full* + reg2full + xfr
full = reg1full x reg2full
empty = reg1full* x reg2full*



data buffer registers

inputis 1

route2A1

reg1last

reg1full

reg 1

outputis 1

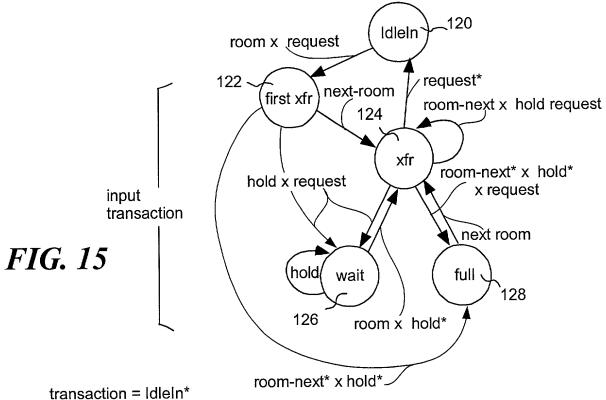
route2A2

reg2last

reg2full

reg 2

FIG. 14

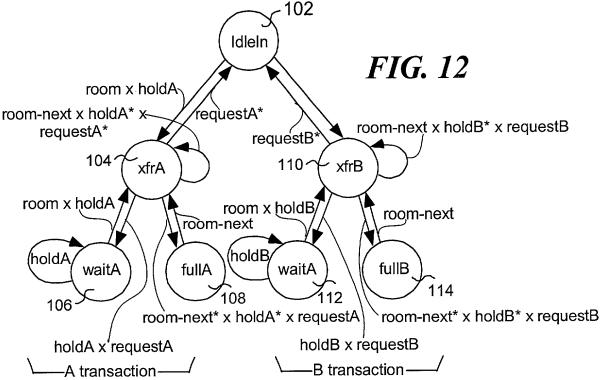


transaction = IdleIn*
room-next = empty + xfrA + xfrB
room = reg1full* + reg2full* + xfrA + xfrB
full = reg1full x reg2full
empty = reg1full* x reg2full*

output-islast x (xfrA + xfrB) x full*

req-out 132

print, with print, 35 (1994, 50 (1994, 1996, 1996, 1996, 1996, 1996, 1997, 199



transaction = IdleIn*
room-next = empty + xfr
room = reg1full* + reg2full + xfr
full = reg1full x reg2full
empty = reg1full* x reg2full*

output-islast x xfr x full*

req-out 118

xfrA + xfrB

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register management flip-flops

data buffer registers

inputis 1 ro

route2A1 reg1last

reg1full reg 1

outputis 1

route2A2

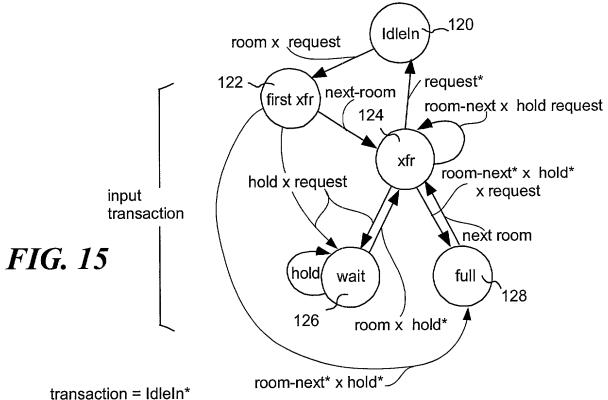
reg2last

reg2full

reg-1

reg z

FIG. 14



room-next = empty + xfrA + xfrB room = reg1full* + reg2full* + xfrA + xfrB full = reg1full x reg2full empty = reg1full* x reg2full*

output-islast x (xfrA + xfrB) x full*

FIG. 16

| Total Continuous Continuous